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10/757,974	01/15/2004	Jenoe Tihanyi	1890-0033	4260

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,974	TIHANYI, JENOE	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15 and 18-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15 and 18-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 04-26-06. Applicant' arguments with respect to the 112, 2nd problem have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remain rejected under Alessandria et al. However, the rejection changes slightly for clarification. New ground of rejections necessitated by the amendment and newly added claims is set forth below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15 and 17-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alessandria et al. (US 2003/0006892A1) in view of Kimura (USP. 6,851,849), Hartwick (USP. 4,881,024), Kumar (USP. 6,855, 981), Zeiler (USP. 4,937,470) and Pavlin (USP. 5,438,286). See attached paper.

Regarding claim 15, figure 10 of Alessandria shows a MOSFET circuit comprising: a first MOS transistor (23), a second MOS transistor (22) connected in parallel, a Zener diode (20) coupled between the gates of the first and second MOS transistors. Figure 2 of Pavlin shows a MOSFET circuit comprising a first transistor (TP1) and a second transistor (TP2) wherein the second transistor has less cells than the first transistor (col. 3, lines 32-50). The circuit taught by Pavlin has lower threshold current (IL) than the circuit having two transistors having an equal number of cells (col. 4, lines 41-62). Therefore, it would have been obvious for one of ordinary skill in the art to replace transistors (22) and (23) of Alessandria with the transistors taught by Pavlin for lowering the threshold current (total IL) thus, the power consumption of the circuit is reduced.

Regarding claims 19 and 18, the combination of Alessandria and Pavlin includes all the limitation of these claims except for the limitation that the circuit further comprises a first resistor connected in parallel with the Zener diode. The circuit of circuit of Alessandria has a limitation that the voltage applied to the gate of transistor (T2) only happens when the input voltage (Vin) is high enough to reverse biased Zener (20). Figure 1 of Zeiler shows a Zener diode (44) having a resistor (46) coupled in parallel with it for continuously controlling the second MOS transistor (T2) and for limiting the voltage applied to the gate of the second MOS transistor. Therefore, it would have been obvious for one of ordinary skill in the art to replace the single diode (20) of Alessandria with the diode and the resistor taught by Zeiler for continuously controlling the second MOS transistor (T2) and for limiting the voltage applied to the gate of the second transistor. The second resistor is resistor (R2).

Regarding claim 20, the combination of Alessandria, Pavlin and Zeiler includes all the limitations of claim 20 except for the limitation that that the zener diode (44) and the resistor (46) of Zeiler are integrated with one another for having a compact circuit.
It is old and well known that the components of an integrated circuit are fabricated on a piece of silicon. Therefore, it would have been obvious for one of ordinary skill in the art to integrate the zener diode (44) with the resistor (46) for having a compact circuit.

Regarding claims 21, 22, 23 and 32, the technique of fabrication of the zener diode and the resistor are well known in the art and is fully shown by Kumar (6,855, 981, col. 11, lines 24-30). Kumar does not show that "the dope concentration of the highly doped layer is less than 10exp 19 charge carrier cm –exp 3". However, it is old and well known and it would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative predetermined value of a differential input voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative predetermined value of a differential input voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in

concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990) as set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one having ordinary skill in the art to select the dope concentration of the highly doped layer to be less than 10exp19 charge carrier cm –exp 3" dependent upon particular environment of use to ensure optimum performance.

Regarding claims 24, figure 10 of Alessandria shows a MOSFET circuit comprising: a first MOS transistor (T1), a second transistor (T2) coupled in parallel with the first MOS transistor, a constant voltage element is a Zener diode (20). Figure 10 of Alessandria does not show that the first MOS transistor has a first number of cells and the second MOS transistor has a second number of cells. Figure 2 of Pavlin shows a MOSFET circuit comprising first second MOS transistor (TP1) and second NMOS transistor (TP2) coupled in parallel. The second transistor (TP2) has a second number of cells less (10-40 times) than the first number of cells (col. 4, lines 35-40) for providing a circuit having low threshold current (IL) that is many times lower than the circuit of Alessandria wherein the transistors have an equal number of cells (col. 4, lines 41-62). Therefore, it would have been obvious for one of ordinary skill in the art to replace transistors (T1) and (T2) of Alessandria with the transistors taught by Pavlin for lowering the threshold current (total IL) thus, the power consumption of the circuit is reduced. The resistor is element (R2).

Regarding claims 25-27 and 29, the first number of cells is 10 to 40 times larger than the second number of cells (col. 4, lines 35-40). The first number of cells is from 15,000 to 20,000 (col. 4, lines 38-40).

Regarding claim 28, transistors (TP1) and (TP2) of Pavlin constitute a main composite transistor (TP) that is used to compensate the threshold current by lowering it X times lower (col. 4, lines 50-62).

Regarding claims 30, figure 10 of Alessandria shows a MOSFET circuit comprising: a first MOS transistor (T1), a second transistor (T2) coupled in parallel with the first MOS transistor, a constant voltage element is a zener diode (20). Figure 3 of Alessandria does not show that the first MOS transistor has a first number of cells and the second MOS transistor has a second number of cells. Figure 2 of Pavlin shows a MOSFET circuit comprising first second MOS transistor (TP1) and second NMOS transistor (TP2) coupled in parallel. The second transistor (TP2) has a second number of cells less (10-40 times) than the first number of cells (col. 4, lines 35-40) for providing a circuit having low threshold current that is many times lower than the circuit of Alessandria wherein the transistors have an equal number of cells. (col. 4, lines 50-62). Therefore, it would have been obvious for one of ordinary skill in the art to replace transistors (T1) and (T2) of Alessandria with the transistors taught by Pavlin for lowering the threshold current (total IL) thus, the power consumption of the circuit is reduced.
The resistor is element (R2). Even though, Alessandria does not mention that the zener diode is fabricated with a technique recited in claim 30. However, this technique is a common technique shown in US Pat. 6,855,981, col. 11, lines 23-44.

Regarding claim 31, the resistor is element (R2). Kuma col. 11 shows that the resistor can be formed by the pn junction between the polycrystalline layer and the zone.

Regarding claims 33 and 34, the first number of cells is 10 to 40 times larger than the second number of cells (col. 4, lines 35-40). The first number of cells is from 15,000 to 20,000 (col. 4, lines 38-40).

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alessandria et al. (US 2003/0006892A1) in view of Pavlin (USP. 5,438,286), Lecce et al. (US 5,917,254) and Rademaker et al. (US 5,359,655).

Regarding claim 35, the combination of Alessandria and Pavlin includes all the limitations of this claim except for the limitation that the zener diode is forward biased from the control input to the gate of the gate of the second MOS transistor. Figures 3 of Lecce shows a zener diode connected reverse bias for setting a threshold for the gate of the transistor. Figure 1 of Rademaker shows a zener diode connected forward bias for setting a

higher threshold for the gate of the transistor. It is old and well known to one of ordinary skill in the art that when a zener diode is forward bias, the voltage drop across it is smaller than the voltage drop across the zener diode when it is reversed biased. Therefore, the forward bias of the zener diode for raising the threshold voltage applied to the gate of second MOS transistor is considered to be design expedient depending upon a particular environment or an application in which the circuit of Alessandria is to be used. Lacking of showing any criticality, a skilled artisan would be motivated to forward bias diode (20) of Alessandria for raising the threshold voltage applied to the gate of transistor (T2).

Response to Arguments

In the Remarks, the Applicant argues that:

a. there is no legally sufficient motivation or suggestion to combine Alessandria and Pavlin.

b. the Examiner's application of Alessandria contains inadvertent errors.

In the previous Office Action, **only figure 10** of Alessandria was used for the rejection. In figure 10, the so-called transistor (23) was not previously labeled. For easy interpretation of figure the Examiner labeled that transistor as (23). This label (23) is not related to element 23 of figure 5. To avoid misunderstanding, transistors (23) and (22) are relabeled as (T1) and (T2).

Alessandria shows a circuit that is similar to the circuit of the present application except for the limitation that the second transistor (T2) has less cells than the first number of cells of the first transistor (T1). Figure 2 of Pavlin shows a first transistor (TP1) having a source-drain path in parallel with the source-drain path of the second transistor (TP2). Transistor (TP2) has a number of cells less than the number of cells of transisitor (P1) (col.4, lines 35-40). Because of the difference of cells between two transistors, the threshold current, the total current (IL), is lower than the total current of a circuit having two transistors that have equal number of cells (col. 4, lines 41-62). Because the total current is reduced, the power consumption and the heat generated by the circuit are reduced. In conclusion, the circuit of claim 15 fully reads on the combination of Alessandria and Pavlin and the motivation in this rejection is legally proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
07-14-06

TUAN T. LAM
PRIMARY EXAMINER